A Reconfigurable Time-Domain Comparator for Multi-Sensing Applications

Xiaopeng Zhong, Bo Wang and Amine Bermak, Fellow, IEEE
ECE Department, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong
Email:{xzhongab, vandy, eebermak}@ust.hk

***Abstract*—Wireless sensor network applications typically include various sensors (temperature, humidity, gas, etc.) and each sensor has different requirements of speed, noise, offset, and power consumption. In order to optimize the performance and allow long-time operation, reconfigurability is mostly desirable in the readout circuitry. In this paper, a reconfigurable time-domain comparator (RTDC) with low noise and low offset is proposed, mainly for reconfigurable SAR ADCs in wireless sensor nodes. With a supply voltage of 1.8 V, it can be dynamically reconfigured to operate in seven different modes for different sensing scenarios. From Mode 1 to Mode 7, the maximum operating speed of the comparator ranges from 182 MHz to 20 MHz with its input referred noise been reduced exponentially from 142 μV to 63.4 μV and its offset been reduced exponentially from 7.64 mV to 2.55 mV, respectively. The simulated energy efficiency is 1.27 pJ/conv in Mode 1 and it linearly increases to 9.48 pJ/conv in Mode 7. This wide operating range enables the best possible trade-off for the sensing node application at hand.**

I. Introduction

Wireless sensor network has drawn much attention in recent years and it has led to emergence of new application areas such as environmental monitoring, health care and manufacturing process monitoring. As the sensing nodes are closely interacting with the environment, the sensing devices are exposed to extreme conditions and unknown and unpredictable dynamics. In addition, sensing nodes may include heterogenous set of sensing devices with different readout requirements (speed, noise, offset, power, etc). Using a single readout circuit to interface various sensors is desirable for low-cost applications but very challenging due to diverse performance requirements such as varying bandwidth, different dynamic range and resolution. Furthermore, wireless sensor device is always energy constrained so that energy-efficient design must be taken into special consideration. As a result, sensor readout circuitry for low cost sensor network applications need to adaptively reconfigure its operation depending on the sensor being accessed and changes in the environment; leading to the so-called adaptive reconfigurable sensing node.

Sensors typically output analog signals as the sensed environment is analog while data processing is performed in digital domain with mature Digital Signal Processing (DSP) techniques. Analog-to-digital converters (ADCs) are therefore very important building blocks as they enable the sensing device to interface with the DSP hardware. ADCs in wireless sensing device will have to deal with various bandwidth and noise requirements of signals, and also operate autonomously for extended period of time. Thus reconfigurability is desirable in the design of ADC to meet the dynamics of sensors' signals and avoid unnecessary power consumption. Among different architectures of ADCs, successive approximation register (SAR) are preferably used for sensor devices due to its high energy efficiency, moderate resolution and flexible structure [1][2][3][4]. SAR ADC relies on its comparator to achieve targeted speed, noise, offset and power consumption metrics. Reconfigurable SAR ADCs [1][2] to date have focused on DAC design while neglecting the comparator which can consume comparable if not larger amount of power within the DAC for a given resolution [3][4].

Regenerative StrongArm comparator and double-tail latch type comparator are commonly used in the design of SAR ADC due to their high speed and power efficiency [1][2][3][4]. However, these reported comparators suffer from large offset (tens of mV) and large noise (hundreds of μV) thus special techniques are needed to reduce the effect of offset and noise [5][6], which not only increases the cost but also limits the reconfigurability of the comparator. As an alternative approach, time-domain comparators were proposed [7][8][9][10]. Nevertheless, the previously proposed time-domain comparators are not reconfigurable and hence not suitable for wireless sensor network featuring multi-sensing and single read-out platform.

This paper presents a reconfigurable time-domain comparator (RTDC) for reconfigurable SAR ADC that can be deployed for wireless sensor network with multi-sensing and single read-out platform. It can be dynamically reconfigured to meet different application or readout requirements under varying sensing conditions.

The remainder of this paper is organized as follows. Section II presents the operation principle of the RTDC. Section III provides the comparator implementation. Section IV reports the simulation results of the RTDC in terms of speed, noise, offset and power consumption. Finally a conclusion is drawn in Section V.

II. Operation Principle

The comparator is shown in Fig.1. It consists of two reconfigurable voltage controlled delay lines (RVCDLp, RVCDLn), two 7-to-1 multiplexers (MUXp, MUXn) and a phase detector (PD). Each RVCDL has seven serially connected unit delay stages ($D1$-$D7$) and one or more of them can be disconnected from the delay chain as controlled by $ctl[7:1]$ (decoded from $set[2:0]$). The multiplexers, which are also controlled by $set[2:0]$, then select one out of the seven outputs

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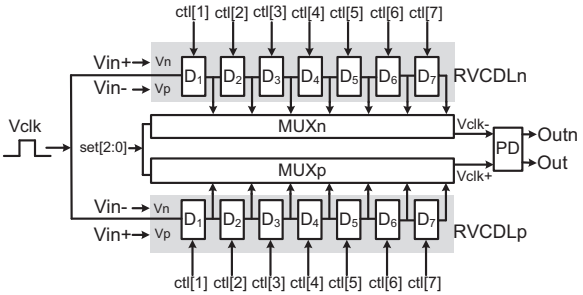
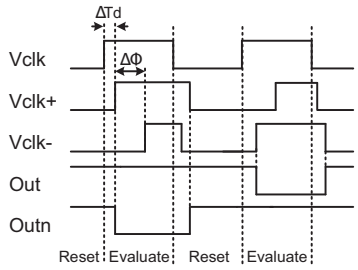


(a)



(b)

Fig. 1. (a) Topology and (b) timing diagram of the proposed reconfigurable time-domain comparator (RTDC).

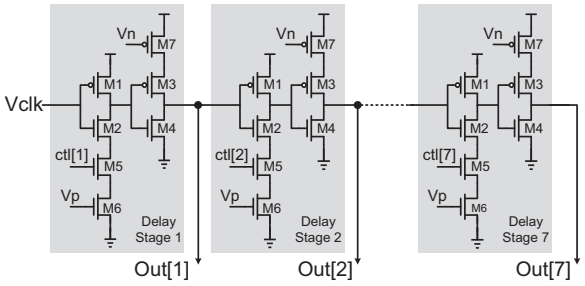


Fig. 2. Implementation of the reconfigurable voltage controlled delay line (RVCDL) of RTDC.

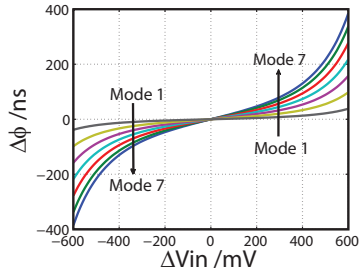


Fig. 3. Relationship between propagating signal phase difference $\Delta\phi$ and input voltage difference ΔV_{in} (V_{in+} and V_{in-} have a common mode voltage of $V_{DD}/2$).

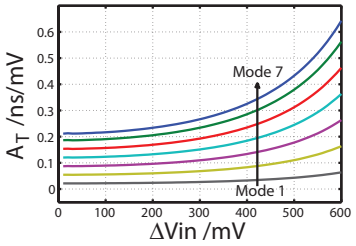


Fig. 4. Voltage-to-Phase Gain A_T of the RVCDLs (symmetrical along y-axis).

from RVCDLp and RVCDLn, respectively. The phase detector compares the phase difference between the two output signals from the multiplexers and gives the comparison result.

During operation, when the input clock signal V_{clk} is low, the whole comparator is reset. When V_{clk} becomes high, since the propagation speeds of V_{clk} in RVCDLp and RVCDLn are controlled by the comparator's input voltages V_{in+} and V_{in-}, the signals V_{clk+}, V_{clk-} have different delays compared to V_{clk}. As a result, the input voltage difference between V_{in+} and V_{in-}, in voltage-domain, is converted into a phase difference $\Delta\phi$ between V_{clk+} and V_{clk-}, in time-domain. Unlike the reported time-domain comparators [7][8][9][10], this comparator can be dynamically reconfigured to meet the specific requirements of different application scenarios, including speed, noise, offset and power, as analyzed in Section III and IV.

III. Circuit Implementation

A. Delay Stage

The implementation of the delay chain for this time-domain comparator is shown in Fig.2. Each delay stage consists of two current-starved inverters (M1-M2, M3-M4) with V_p controls the discharging current I_p flowing through M1-M2 and V_n controls the charging current I_n flowing through M3-M4. Notice that given the same common mode voltage V_{com}, if V_p is larger than V_n, the unit delay t_d is shorter as both I_p and I_n are larger, and vice versa. In the delay stage, an NMOS switch M5 is inserted into the first inverter thus the corresponding delay stage D_i can be excluded from the RVCDL if $ctl[i]$ is disabled.

Fig.3 shows the relationship between the phase difference $\Delta\phi$ between V_{clk+} and V_{clk-} and the input voltage difference ΔV_{in} between V_{in+} and V_{in-}. The voltage-to-phase gain of the RVCDL can be approximated as [8]:

$$A_T = \frac{\Delta\phi}{\Delta V_{in}} \propto N \cdot \frac{C_L \cdot V_{DD}}{G_m(V_{com}^2 - \Delta V_{in}^2)} \quad (1)$$

where N is the number of delay stages enabled in the RVCDL; C_L is the overall equivalent load capacitance of the two inverters of the unit delay stage; V_{DD} is supply voltage and G_m is the average transconductance of M6 and M7. Indicated by (1), A_T can be increased by either increasing C_L or reducing G_m. The relationship between A_T and ΔV_{in} is shown in Fig.4. It indicates that larger ΔV_{in} and N yield larger A_T, which is consistent with (1).

In this design, M1-M2 and M3-M4 are large transistors so as to obtain a large C_L. The simulated output capacitances are 27.63 fF and 34.67 fF for the inverters formed by M1-M2 and M3-M4, respectively. M6-M7 with small W/L (width/length) ratios are used to control the transient currents and for small G_m, thereby further boost A_T. Moreover, as the transistor mismatches between the two RVCDLs directly

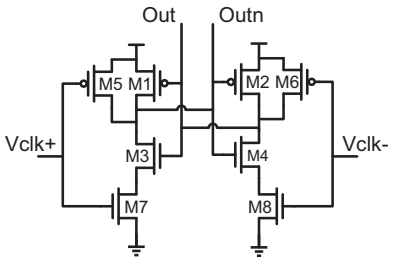
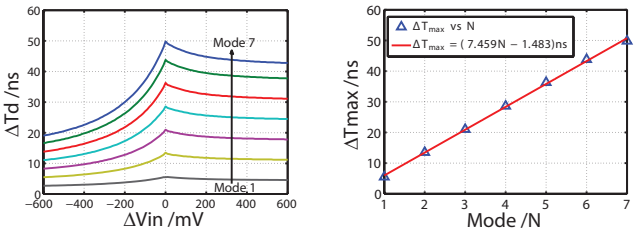


Fig. 5. Circuit implementation of the phase detector of RTDC.



(a) (b)

Fig. 6. Simulated (a) time delay ΔT_d between the comparator output $Out/Outn$ and the input clock signal V_{clk} of RTDC and (b) the maximum time delay ΔT_{dmax} in different operation modes.

affect the comparator's offset, especially M6-M7 that control the transient currents, their transistors sizes (width and length) are proportionally scaled to have a larger area.

B. Phase Detector

In this design, a NAND latch is adopted as the phase detector for fast operation as well as power saving. The circuit implementation of the phase detector is shown in Fig.5. In the reset phase, V_{clk+} and V_{clk-} are '0' and reset Out and $Outn$ to be '1'. During the evaluation phase, M7-M8 are turned on while M5-M6 are turned off. The latch (M1-M3, M2-M4) makes decision based on first coming signal and decides the state of the following SR latch. For example, if the rising edge of V_{clk+} arrives first, Out will be '1' and vice versa.

During the reset phase of the comparator (V_{clk}=0), since V_p and V_n are still controlling the tail-currents by M6-M7, respectively, the output node of each inverter has both discharging current and charging current. If V_{in+} is larger than V_{in-}, V_{clk+} (RVCDLp) will reset slower than that of V_{clk-} (RVCDLn) and vice versa, as shown in Fig.1(b). This non-overlapping phase avoids malfunction during the reset phase and protects the comparison result.

IV. Simulation Results

The RTDC is designed and simulated in the Global-Foundries 0.18 μm mixed signal CMOS process. Its speeds, noises, offsets and power consumptions are characterized under different configurations.

A. Speed

As illustrated above, the phase difference $\Delta\phi$ between V_{clk+} and V_{clk-} determines the input sensitivity of the comparator. However, in order to determine the maximum operating speed of the comparator, the time delay ΔT_d between the comparison output $Out/Outn$ and the input clock signal V_{clk} needs to be identified. As shown in Fig.6(a), ΔT_d changes with ΔV_{in}. When $|\Delta V_{in}|$ increase, ΔT_d decreases because both I_p and I_n becomes larger, making the whole comparator faster. Notice that ΔT_d is dominated by the RVCDLs as the delay of phase detector is only 48.05 ps.

The maximum delay ΔT_{dmax} are simulated with V_p=V_n=$V_{DD}/2$ and is plotted in Fig.6(b), where ΔT_{dmax} ranges from 5.48 ns to 49.8 ns. The fitted curve between ΔT_{dmax} and the operation mode (N) shows that each delay stage equally adds a delay of 7.459 ns to the comparator, thereby the comparator speed is decreasing from Mode 1 to Mode 7. Based on T_{max}, the maximum operating frequency (F_{max}) of the RTDC is reconfigurable from 182 MHz in Mode 1 down to 20 MHz in Mode 7.

B. Noise

In the RVCDLs, each delay stage contributes certain phase noise to the outputs V_{clk+}, V_{clk-} of the delay chains. The total time-domain noise power of the RTDC is expressed as [10]

$$\overline{\phi}_{ni}^2 = 2N \cdot (A_t \cdot \overline{v}_{ni})^2 \tag{2}$$

where A_t is the voltage-to-phase gain of each delay stage and $\overline{v}_{ni}$ is the input referred noise of a unit delay stage. The noise effect of the PD is neglected since it has a small input referred voltage-to-phase gain. Thereby the input referred noise of the RTDC is

$$\overline{V}_{ni} = \frac{\overline{\phi}_{ni}}{N \cdot 2A_t} = \frac{\overline{v}_{ni}}{\sqrt{2N}} \tag{3}$$

It shows that the equivalent noise of the RTDC equals the noise of a unit delay stage attenuated by $\sqrt{2N}$. Different from conventional comparators that have no noise attenuation or limited by the noise from pre-amplifier, the time-domain comparator possesses the advantage of noise averaging.

The comparator noise is simulated by transient noise analysis with $V_{in-} = V_{DD}/2$ and V_{in+} sweeping around V_{in-}. The RMS noise of the input referred noise V_{ni} (1σ value) is calculated by fitting the simulated results to a normal cumulative distribution. In Fig.7(a), the fitting equation between V_{ni} (1σ value) and N is $V_{ni} = 212/\sqrt{2N}\mu V$, indicating the maximum noise (N=1) for this comparator is about 150 μV. Compared with conventional comparators whose noises always exceed hundreds of μV [11][12], this comparator has a lower noise level for all seven modes.

C. Offset

Similar with the analysis of the comparator noise, since the input referred offset (v_{os}) of each delay stage is uncorrelated, the total phase offset of the RTDC is $\sqrt{2N} \cdot A_t \cdot v_{os}$. Therefore, the input referred offset of the RTDC is expressed as

$$V_{os} = \frac{\sqrt{2N} \cdot A_T \cdot v_{os}}{N \cdot 2A_T} = \frac{v_{os}}{\sqrt{2N}} \tag{4}$$

which is also attenuated down by a factor of $\sqrt{2N}$. V_{os} is simulated for different operation modes with Monte Carlo simulation (200 runs). As shown in Fig.7(b), V_{os} decreases from

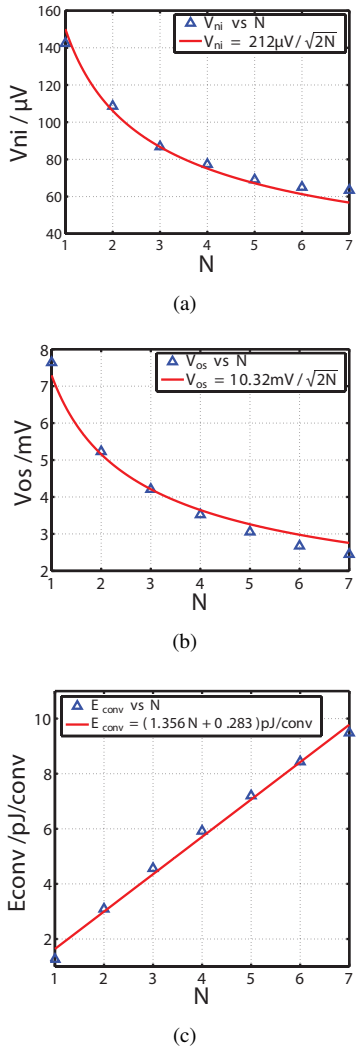


Fig. 7. Simulated (a) input referred noise, (b) input referred offset and (c) power consumption of RTDC in seven operation modes.

7.64 mV in Mode 1 to 2.55 mV in Mode 7. The relationship between V_{os} and N is fitted to be $V_{os} = 10.32/\sqrt{2N}mV$. Compared with conventional comparators whose offsets are in the order of tens of mV [5][6], this design achieves an offset level which is less than 10 mV. V_{os} in Mode 7 is even comparable to those offset-calibrated comparators [5][6].

D. Power

The dynamic power consumption of the inverters in the RVCDLs dominates the overall comparator power. Fig.7(c) indicates that total energy consumed per conversion E_{conv} is linearly proportional to N. E_{conv} ranges from 1.27 pJ/conv to 9.48 pJ/conv for the seven operation modes. Fitting result shows that each delay stage consumes about 1.36 pJ/conv.

V. Conclusion

A reconfigurable time-domain comparator (RTDC) is presented, with its main specifications listed in Table I. It features low noise and low offset because of the noise and offset averaging characteristics of this topology. The speed, noise, offset and power of the designed comparator can be dynamically reconfigured to meet the specific application requirements of SAR ADC in multi-sensing platform. Based on the practical requirements, more delay stages can be added to enhance its reconfigurability and to achieve the target performance.

TABLE I
Operation Specifications of RTDC

Mode (N)	set[2:0]	Fmax/ MHZ	Noise/ μV	Offset/ mV	Power/ pJ/conv
1	001	182	142	7.64	1.27
2	010	74	109	5.23	3.09
3	011	47	85.7	4.21	4.56
4	100	34	77.3	3.52	5.92
5	101	27	69.9	3.05	7.20
6	110	22	65.0	2.68	8.43
7	111	20	63.4	2.55	9.48

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